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EXAMINER	
NADAV, ORI	
ART UNIT	PAPER NUMBER
2811	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/654,845	Applicant(s) HAO ET AL.	
	Examiner ori nadav	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2002* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *18-34* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schlangenotto et al. (5,063,428) in view of Schlangenotto et al. (5,773,858, cited by applicant).

Regarding claim 1, Schlangenotto et al. (5,063,428) teach in figure 6 and related text a power semiconductor device having high avalanche capability, the device comprising: an N+ doped layer 4 and, in sequence, N doped 3, P doped 2a, and P+ doped 2b (column 6, line 64 column 7, line 3 and figure 4) semiconductor layers.

Although figure 6 of Schlangenotto et al. (5,063,428) does not depict "N-" 3 and "P-" 2a semiconductor layers, N doped 3 and P doped 2a semiconductor layers are "N-" and "P-" semiconductor layers, because the concentration of N doped 3 and P doped 2a semiconductor layers (figure 9) is the same or lower than that of the N- and P- doped semiconductor layers of the claimed invention. Therefore, Schlangenotto et al. (5,063,428) teach "N-" and "P-" doped semiconductor layers, as claimed.

Although Schlangenotto et al. (5,063,428) do not categorize N+ doped layer 4 as a substrate, N+ doped layer 4 is the base layer for N doped 3, P doped 2a, and P+ doped 2b semiconductor layers, which are formed there over. Therefore, N+ doped layer 4 can be categorized as a substrate, as claimed.

Schlangenotto et al. (5,063,428) do not teach in the embodiment of figure 6 P- doped 2a and P+ doped 2b layers having a combined thickness of about 5 microns to about 12 microns and recombination centers comprising noble metal impurities disposed substantially in the N - doped and P- doped layers.

Regarding the claimed limitations of P- doped 2a and P+ doped 2b layers having a combined thickness of about 5 microns to about 12 microns, Schlangenotto et al. (5,063,428) teach that the P- doped 2a and P+ doped 2b layers have a doping curve similar to that of figure 4 (column 7, lines 3-5). Schlangenotto et al. (5,063,428) further teach P+ doped layer 2b having a thickness of 0.2 microns (column 5, lines 33-35), wherein P- doped layer 2a should have a thickness greater than 5 microns and less than 70 microns (column 5, line 65 to column 6, line 3). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use P- doped 2a and P+ doped 2b layers having a combined thickness of about 5 microns to about 12 microns, in the device of Schlangenotto et al. (5,063,428) in order to form a device as small as possible within the criteria limits of Schlangenotto et al. (5,063,428). Note that at the time the claimed invention was made (12 years after the device of Schlangenotto

et al. (5,063,428) was formed), the size of semiconductor devices has been dramatically minimized.

Regarding the claimed limitations of forming recombination centers comprising noble metal impurities disposed substantially in the N - doped and P- doped layers, Schlangenotto et al. (5,063,428) teach that it is known in the art to form recombination centers comprising noble metal impurities in power diodes in order to reduce charge carrier life (column 1, lines 24-29). Schlangenotto et al. (5,063,428) further teach forming recombination centers in the power diode of figure 3 in order to improve the characteristics of the device (column 5, lines 39-46).

Schlangenotto et al. (5,773,858) teach that it is known to form recombination centers in high speed power diodes in order to improve the dynamic characteristics by lowering the charge carrier life (column 1, lines 21-25).

Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) do not limit the location of the recombination centers to specific areas of the power diodes. Therefore, it is understood to an artisan that the recombination centers are formed throughout the power diodes.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form recombination centers comprising noble metal impurities in the device of Schlangenotto et al. (5,063,428) in order to order to improve the dynamic characteristics of the device by lowering the charge carrier life by a well known method. The combination is motivated by the teachings of Schlangenotto et al. (5,063,428) and

Schlangenotto et al. (5,773,858) who point out the advantages of forming recombination centers in power diodes. Note that the broad recitation of the claim does not require the recombination centers to be located only in the N - doped and P- doped layers. Regarding the claimed limitations of a power semiconductor device having high avalanche capability, this feature is inherent in the device of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858), because the device of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) comprises recombination centers, and the avalanche capability is a function of the recombination centers.

Regarding claim 2, Schlangenotto et al. (5,063,428) do not teach a P- doped 2a layer having a thickness of about 4 microns to about 10 microns. it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use P-doped 2a layer having a thickness of about 4 microns to about 10 microns in the device of Schlangenotto et al. (5,063,428) in order to form a device as small as possible within the criteria limits of Schlangenotto et al. (5,063,428).

Regarding claim 3, Schlangenotto et al. (5,063,428) teach P+ doped layer 2b having a thickness of about 0.1 to about 2 microns (column 5, lines 33-35)

Regarding claims 4-5 and 7, Schlangenotto et al. (5,063,428) do not teach a P- doped layer has a dopant level of at least 10E16 atoms/cm3 and a dopant level of about 2.5x

10E17 atoms/cm3 and a P+ doped layer has a dopant level of about 6x10E19 atoms/cm3, respectively. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a P- doped layer having a dopant level of about 2.5x 10E17 atoms/cm3 and a P+ doped layer has a dopant level of about 6x10E19 atoms/cm3 in the device of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858), since forming a P- doped layer having a dopant level of about 2.5x 10E17 atoms/cm3 is within the skills of an artisan, subject to routine experimentation and optimization. Note that differences in concentration or temperature do not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller , 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele , 406 F.2d 1403, 160 USPQ 809 (CCPA 1969). For more recent cases applying this principle, see Merck & Co. Inc . v. Biocraft Laboratories Inc. , 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied , 493 U.S. 975 (1989), and In re Kulling , 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990).

Regarding claim 6, Schlangenotto et al. (5,063,428) teach in figure 9 a P+ doped layer has a dopant level of at least 1018 atoms/cm3.

Regarding claim 8, Schlangenotto et al. (5,063,428) teach in figure 9 an N -doped layer having a dopant level of about 10E14 atoms/cm3. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an N- doped layer having a dopant level of about 10E14 atoms/cm3 to about 10E15 atoms/cm3 in the device of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858), since forming an N -doped layer having a dopant level of about 10E14 atoms/cm3 to about 10E15 atoms/cm3 is within the skills of an artisan, subject to routine experimentation and optimization.

Regarding claim 9, Schlangenotto et al. (5,773,858) teach a power diode formed in epitaxial layers (column 9, line 27). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form N- doped, P- doped, and P+ doped semiconductor layers as epitaxial layers in the device of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858), in order to have more control over the thickness of the layers and to obtain better quality layers.

Regarding claims 10-11, Schlangenotto et al. (5,063,428) teach noble metal impurities comprise platinum (column 1, lines 26-27).

Regarding the process limitations recited in claim 12 ("recombination centers are formed by platinum diffusion through the N + doped substrate"), these would not carry

patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced. Note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Fessmann, 180 USPQ 324; In re Avery, 186 USPQ 161; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and In re Marosi et al., 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 13-14, Schlangenotto et al. (5,063,428) do not teach platinum impurities at a concentration of about 1x10E15 to about 1x10E16 atoms/cm3, and about 2x1015 atoms/cm3. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form platinum impurities at a concentration of about 1x10E15 to about 1x10E16 atoms/cm3, and about 2x1015 atoms/cm3 in the device of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858), in order to adjust the device characteristics according to the requirements of the application in hand, since the reverse current and the device performance depend on the platinum impurities concentration.

3. Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858), as applied to claim 1 above, and further in view of Tokura et al. (5,545,908).

Regarding claims 15-17, Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) teach substantially the entire claimed structure, as applied to claim 1 above, except using the power diode in a MOSFET or an IGBT power device, wherein an N+ doped region disposed in the N -doped layer, adjacent the P+ and P- doped layers. Tokura et al. teach in figure 1 using a diode in a MOSFET or an IGBT power device, wherein an N+ doped region 7 disposed in an N -doped layer 2, adjacent P+ 10 and P- 8 doped layers. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the power diode of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858), in a MOSFET or an IGBT power device, wherein an N+ doped region disposed in the N- doped layer, adjacent the P+ and P- doped layers in order to use the advantages of the power diode of Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) in an application which requires a MOSFET power device.

Response to Arguments

4. Applicant argues that reducing the size of the device means reduction in the width and length of the device and it does not mandate reduction in the thickness of the layers.

Reduction in the width and length of the device mandates a reduction in the thickness of the layers of the device, because the width and length of the device comprises layers. When the width and length of the device are reduced, the thickness of the layers is proportionally reduced. Therefore, reducing the width and length of the device mandates a reduction in the thickness of the layers.

5. Applicant argues that prior art does not teach recombination centers formed in the N - doped and P- doped layers.

Schlangenotto et al. (5,063,428) and Schlangenotto et al. (5,773,858) do not limit the location of the recombination centers to specific areas of the power diodes. Therefore, it is understood to an artisan that the recombination centers are formed throughout the power diodes. Thus, the recombination centers are also formed in the N - doped and P- doped layers, as claimed.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.

Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to *Examiner Nadav* whose telephone number is **(703) 308-8138**. The Examiner is in the Office generally between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday. If attempts to reach the examiner by

telephone are unsuccessful, the examiner's supervisor, Tom Thomas, can be reached at **(703) 308-2772.**

Any inquiry of a general nature or relating to the status of this application should be directed to the **Technology Center Receptionists** whose telephone number is **308-0956**

Ori Nadav
May 9, 2003

ORI NADAV
PATENT EXAMINER
TECHNOLOGY CENTER 2800